

# FPGA Design and Simulation Made Easy



## Active-HDL™

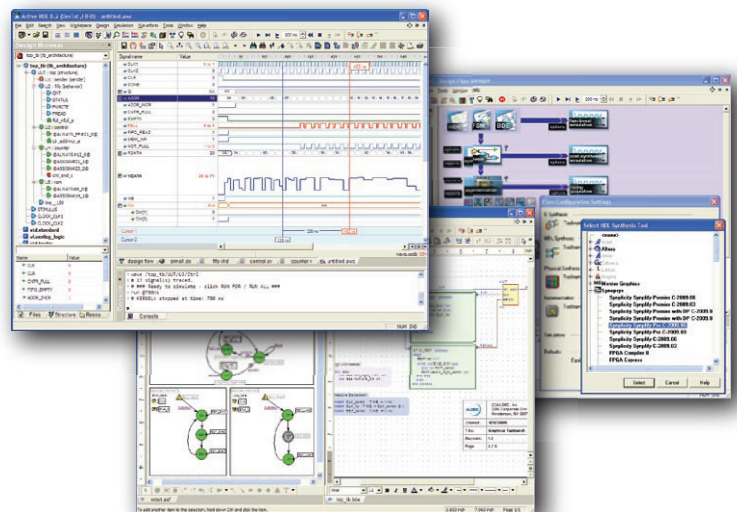
Active-HDL is an integrated FPGA Design and Simulation solution, with design entry, a high-performance mixed-language simulator and an easy-to-use, multi-vendor FPGA flow manager that controls Simulation, Synthesis and Implementation for industry leading FPGA devices, from Actel™, Altera®, Lattice®, Quicklogic® and Xilinx®. Active-HDL has interfaces to over 80 leading EDA tools, making it the most powerful environment.

## Top Features

- Graphical Design Entry
- High Performance Mixed-Language RTL Simulator
- IEEE VHDL, Verilog®, SystemVerilog (Design), SystemC
- Advanced Debugging & Code Coverage
- IP Encryption based on IEEE Standards
- Assertion-Based Verification (ABV)
- DSP Co-simulation with MATLAB®/Simulink®
- PCB Design Interface
- HTML and PDF Design Documentation
- Windows® Vista/XP/2003/2000 32/64 bit support

## Graphical Design Entry

Draw any finite state machine diagram and let Active-HDL generate your synthesizable RTL code. Connect all design modules at the top-level and automatically generate output structural HDL using the built-in block diagram editor. If needed, convert HDL to graphics with Code2Graphics™ utility. Active-HDL can also import, re-target, enhance, simulate and debug your legacy designs.



## High Performance, Mixed-Language Simulation

Active-HDL includes a high performance, common-kernel, mixed-language simulator supporting batch mode simulation, VCD, a performance profiler, memory viewer, encrypted IP and FPGA vendor libraries. Drive your system-level simulation model using complex testbenches or create quick and flexible stimulator farms to rapidly test design modules and system-level designs.

## Debugging and Code Coverage

Active-HDL includes state-of-the-art debugging with an Accelerated Waveform, with cross-probing to HDL source code, breakpoint management, testbench and stimulus generation. A powerful HDL code coverage analyzer provides 100% test coverage of all statements, lines, signals, toggle, branch, path and logical expressions in the design.

Visit our website at [www.aldec.com](http://www.aldec.com)

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## STANDARDS



## FEATURES

## PRODUCT CONFIGURATIONS

Design Entry	Designer Edition	PE	EE
HDL, Text, Block Diagram and State Machine Editor	•	•	•
Language Assistant with Templates and Auto-Complete	•	•	•
Macro, Tcl/Tk, Perl script Support	•	•	•
Pre-compiled FPGA Vendor Libraries	•	•	•
Code2Graphics™ Converter		•	•
Legacy Schematic Design Import and Symbol Import/Export		•	•
<b>Supported Languages</b>			
Single or Mixed Language Design Support	Mixed Only	•	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE P1800-2005 (Design)	•	•	•
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0		Option	•
<b>Code Generation Tools</b>			
Testbench Generation from Waveforms		•	•
Testbench Generation from State Diagram		•	•
<b>Project Management</b>			
Design Flow Manager for All FPGA Vendors	•	•	•
Revision Control Interface	•	•	•
<b>Simulation/Verification</b>			
Simulation Performance (Baseline 2X Faster than FPGA Vendor Supplied Simulator)	Baseline	3X Baseline	Up To 6X Baseline
Simulation Model Protection/Library Encryption	•	•	•
VHDL/Verilog IEEE compatible Encryption	•	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•	•
Batch Mode Simulation/Regression (VSimSA)		•	•
Profiler (Performance Metrics)		Option	•
Verilog HDL Simulation Optimization			•
VHDL Simulation Optimization			•
<b>HDL Debug and Analysis</b>			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Memory Viewer	•	•	•
Waveform Viewer (AWF and ASDB) + Editor	Viewer Only	•	•
Waveform Stimulator	•	•	•
Waveform Compare		•	•
Post-Simulation Debug		•	•
C++ Debugger		•	•
Signal Agent (VHDL and Mixed Only)		•	•
X-Trace		Option	•
Advanced Dataflow		Option	•
<b>Coverage Tools Bundle</b>			
Code, Statement, Branch, Expression, Condition, Path and Toggle Coverage		Option	•
<b>Design Rule Checking</b>			
ALINT™ with Aldec Basic Rule Library		Option	•
<b>External Simulation Interfaces</b>			
Synopsys® SmartModels, SWIFT interface and LMTV		Option	•
SpringSoft® Verdi™ PSD mode Interface			•
<b>Co-Simulation</b>			
Simulink® Co-Simulation		•	•
MATLAB® Co-Simulation		Option	•
<b>Assertions</b>			
PSL IEEE 1850 Assertions and Coverage			Option
SystemVerilog IEEE P1800-2005 Assertions and Coverage			Option
OpenVera Assertions and Coverage			Option
<b>Documentation</b>			
Export to PDF/HTML/Bitmap Graphics		•	•
Advanced Export to PDF (Vector Graphics)		•	•
<b>Specialty Solutions</b>			
PCB Interface		•	•
Server Farm Manager		Option	Option
<b>Supported Platforms</b>			
Windows® Vista/XP/2003/2000 32/64 bit	•	•	•



## SILICON



## INTERFACES



### For sales and pricing information contact:

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