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**CADENCE CONTINUES PRODUCT-SEGMENTATION STRATEGY WITH  
ALLEGRO SILICON-PACKAGE-BOARD PLATFORM**

*New Technology in Segmented Allegro Platform Improves Constraint-driven Design Flow and  
Shortens Design Cycle*

**SAN JOSE, Calif. -- April 26, 2006 --** Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced it has extended its product-segmentation strategy to the Cadence® Allegro® system interconnect design platform and is now able to offer a tiered range of products to printed circuit board (PCB) designers. The announcement is the latest in the Cadence product-segmentation strategy to provide customers with multiple levels of technology tailored to specific levels of design complexity. This new release of the Allegro platform offers a range of products scaled to different PCB design complexities and also includes new products, Allegro Design Workbench XL and Allegro Design Publisher XL.

The new Allegro offerings comprise three levels: L, XL and GXL. The Allegro L product series provides PCB design products aimed at solving mainstream design challenges. The Allegro XL product series provides advanced PCB design products that address more complex and high-end design challenges through integrated constraint-driven automation and distributed team-based design productivity. The Allegro GXL product series provides differentiated PCB design products targeting leading-edge design challenges such as advanced package co-design and multi-GHz signal-integrity (SI) analysis.

Allegro Design Workbench XL is a new product that provides component information and library management for Allegro design libraries, automates library revision control and offers a process for distributing known-good libraries including compliance information such as

RoHS to company design centers around the world. This shortens design cycles and reduces component research by up to 50 percent.

“We recognize the need to manage our process as effectively as we manage our data,” said Gary Carter, senior manager for Design Automation at Fujitsu Network Communications. “Cadence’s Allegro Design Workbench allows us to do both. It was easily configured to meet our process and standards, which served to integrate Cadence technology with the other tools we use in our design process. Our engineers also require access to current, complete component information. This includes technical and business data such as cost, lead time and availability, and compliance data for directives such as RoHS. Design Workbench aggregates this information and makes it available to the engineer in one consolidated view.”

Allegro Design Publisher XL enables designs produced with Allegro Design Entry HDL to be published in intelligent, easy-to-navigate PDF files. This provides an easy way for design teams inside and outside the company to review a design without requiring Cadence design entry tools.

With this latest release, a new board-level bus-analysis capability has been added to Allegro PCB SI, shortening time to verify source-synchronous signals used in interfaces such as DDR2 memories. Other enhancements associated with source-synchronous interfaces include support for On-Die Termination (ODT), association of clock, strobe signals to the bus, association of board-level custom stimulus and reports for setup and hold times. In addition, Allegro PCB Editor has been enhanced to shorten the time required to identify critical nets that will potentially have a return path problem.

“The ability to assign custom stimulus with jitter on nets at the board level and to assign different clock speeds to nets has made batch mode analysis of all types of interfaces significantly simpler,” said Kai Keskinen, engineering manager at Celestica. “With set up at board level, the overall simulation of interfaces with source synchronous signals is significantly faster.”

“Designers are increasingly expected to integrate and juggle the multiple requirements of new high-speed interfaces such as PCI Express and DDR2. Our customers are looking for technologies tailored to their specific levels of design needs,” said Charlie Giorgetti, corporate

vice president of marketing for the Allegro and Virtuoso design platforms at Cadence. “This latest release and segmentation of the Allegro platform is another example of how Cadence continues to lead the way in providing well thought out design solutions to the silicon-package-board co-design market segment.”

Allegro is the third Cadence platform to adopt a segmented approach to deliver customer-targeted solutions. In 2005, Cadence introduced tiered ranges of Incisive® functional verification-based products and Encounter® digital IC design products scaled to different design complexities.

Allegro L, XL and GXL will be available in July 2006. People interested in additional details on the latest release of the Allegro platform can register for a Cadence Technology on Tour event near them or contact their local Cadence sales manager.

## **About Cadence**

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics systems. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, printed-circuit boards and systems used in consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2005 revenues of approximately \$1.3 billion, and has approximately 5,000 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at [www.cadence.com](http://www.cadence.com).

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